A1st Final

--72. (new) The method for fabricating the semiconductor integrated circuit according to claim 68,

wherein an N replaces said conductive type P and a P replaces said conductive type N.--

REMARKS

The specification has been amended to make editorial changes including those noted in the Official Action to place the application in condition for allowance at the time of the next Official Action.

Claims 1-36 were previously pending in the application. Claims 1-36 are cancelled and new claims 37-72 are added.

The new claims are believed to address the claim objections and 35 USC §112, second paragraph claim rejections set forth in the Official Action.

The term "longitudinal bipolar transistor" used in the original claims has been changed in the new claims to recite "vertical bipolar transistor". The specification and the claims as originally filed used the terms "longitudinal" and "transverse". One of ordinary skill in the art would interpret these terms to mean "vertical" and "lateral" respectively.

Claims 1, 3, 5, 18-32 and 34-36 are rejected as being anticipated by LI et al. 5,623,387.

Reconsideration and withdrawal of the rejection are respectfully requested because the reference does not disclose or suggest a vertical bipolar transistor formed on a semiconductor substrate and discharging an accumulated electric charge of a pad in a direction from a surface of the semiconductor substrate to a depth of the semiconductor substrate as recited in new claim 37 of the present application.

By way of example, Figure 3 of the present application shows a vertical bipolar transistor having emitter 11 (n^+), base 16 (p^-) and collector 17 (n^-) formed in a depth direction of the semiconductor in a direction from the surface of the semiconductor substrate to a depth of the semiconductor substrate. Base current flows in the base of the vertical bipolar transistor at the surface of the semiconductor substrate. However, the largest amount of current is the collector current which flows in a direction towards collector 17. Therefore, the current does not concentrate at the surface of the semiconductor substrate.

Accordingly, the hot spot in a vertical bipolar transistor due to the collector current is beneath the surface of the semiconductor substrate and the current flows in a vertical

direction, that is in a direction from the surface of the semiconductor substrate along its depth. The width of the flowing current covers the entire area of the emitter. Subsequently, a current dispersion occurs (which means low current density), and the base is not the "hot spot" of the substrate.

In contrast, the base of LI et al. is the hottest spot at the time of current discharge. Specifically, as disclosed on column 11, lines 47-50 of LI et al., the transistor is a lateral bipolar transistor. Accordingly, the collector current flows just below the surface of the substrate as indicated by transistor T124 in Figure 5C of LI et al., for example. LI et al. at column 11, line 60 through column 12, line 3 disclose that the position and shape of Zener diode diffusion region 304 has a second advantage of further channeling current flow in a horizontal direction in the illustration of Figure 5A, avoiding hot spots. This heat dissipation through Zener diode diffusion region 304 is short-lived because as soon as transistor T124 turns on, most current flow is from pad 303 through silicide 302 through resistor R124c in region 305a to the collector of transistor T124 at 305b through the base region of transistor T124 located beneath oxide 306b to resistor R124e in the unsalicided left portion 307a of N+ region 307 to silicide 308 and finally to contact 309.

In this structure, the base becomes the hottest spot at the time of discharging the current so the heat is not easily discharged into a depth direction of the semiconductor substrate. Since the heat is concentrated at the base, of the silicon substrate itself, materials having low dissolving temperature such as the metal wire formed on the substrate, the silicide and the contact will be dissolved by the heat causing a disruption in the current flow.

In an attempt to avoid this problem, column 10, lines 4-10 of LI et al. disclose that to minimize high temperature effects from hot avalanche regions near Zener diode 304, contacts 303 are positioned away from Zener diode 304. In one embodiment, this separation between Zener diode 304 and contacts 303 is about 4 μm. Contacts 303 are also positioned away from the collector-base junction of the transistor, which is beneath field oxide region 306b.

Accordingly, LI et al. teach what is disclosed in the background of the present application of using a lateral bipolar transistor to release the electric current in the lateral direction. LI et al. do not disclose or suggest a vertical bipolar transistor discharging an accumulated electric charge of a pad in a direction from a surface of the semiconductor substrate

to a depth of the semiconductor substrate as recited in claim 37 of the present application.

New claims 38-67 depend from claim 37 and further define the invention and are also believed patentable over LI et al.

In addition, the dependent claims include features not disclosed by the reference. For example, claim 38 recites that a base and a collector of the vertical bipolar transistor are formed in a direction from a surface of the semiconductor substrate to a depth, and an emitter of the vertical bipolar transistor is formed on a surface of the semiconductor substrate. This feature is not disclosed in the reference and thus claim 38 is believed patentable regardless of the patentability of claim 37 from which it depends.

Claims 11, 13, 16 and 17 are rejected as being anticipated by AVERY 5,043,782. This rejection is respectfully traversed.

Claims 11 and 16 are cancelled and claims 13 and 17 are rewritten as claims 54 and 57, respectively and depend from new claim 37, which recites a vertical bipolar transistor formed on a semiconductor substrate and discharging an accumulated electric charge of a pad in a direction from a surface of the semiconductor substrate to a depth of the semiconductor substrate.

Column 3, lines 45-65 of AVERY disclose a lateral bipolar transistor that uses a short base between the collector and emitter. As seen in Figure 2 of AVERY, the emitter 26 and collector 28 are laterally arranged. AVERY does not disclose or suggest a vertical bipolar transistor discharging an accumulated electric charge of a pad in a direction from a surface of a semiconductor substrate to a depth of the semiconductor substrate as recited in claim 37 of the present application. Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

Claims 2, 7, and 33 are rejected as unpatentable over LI et al. in view of MCCLURE et al. 5,774,318. Claims 4 and 6 are rejected as unpatentable over LI et al. in view of A. Sedra and K. Smith textbook, Microelectronic Circuits. Claims 8 and 10 are rejected as unpatentable over LI et al. in view of MCCLURE et al. and further in view of A. Sedra and K. Smith textbook, Microelectronic Circuits. Claim 12 is rejected as unpatentable over AVERY in view of LI et al. Claim 14 is rejected as unpatentable over AVERY in view of LI et al. and further in view of A. Sedra and K. Smith textbook, Microelectronic Circuits. Claim 15 is rejected as unpatentable over AVERY in view of A. Sedra and K. Smith Textbook, Microelectronic Circuits. These

rejections are respectfully traversed.

MCCLURE et al. and A. Sedra and K. Smith Textbook, Microelectronic Circuits do not teach or suggest a vertical bipolar transistor formed on a semiconductor substrate and discharging an accumulated electric charge of a pad in a direction from a surface of a semiconductor substrate to a depth of the semiconductor substrate as recited in claim 37 of the present application. As set forth above, LI et al. and AVERY do not disclose or suggest this feature. Accordingly, the proposed combination of references would not render obvious claim 37 or claims 38-67 which depend therefrom.

New claims 68-72 disclose methods of forming a vertical bipolar transistor. Since none of the disclosed prior art teaches a vertical bipolar transistor, they could not teach or suggest the recited method of forming a vertical bipolar transistor as recited in claims 68-72 of the present application.

An object of the present invention is to use a vertical bipolar transistor as an electrostatic discharge protection circuit for protecting a CMOS inner circuit. The CMOS inner circuit is protected against overvoltage by the vertical bipolar transistor discharging the overvoltage into a direction from the surface of a semiconductor substrate to a depth of the

semiconductor substrate.

As described in the "prior art" section of the present specification, it is known that lateral bipolar transistors are used as ESD protection circuits for discharging overvoltage.

As set forth above, a lateral bipolar transistor is structured to use a surface of the semiconductor substrate as a conductive region. As a result of using a lateral bipolar transistor as an ESD protection circuit, an electric current concentration and an electric field concentration occur on the surface of the semiconductor substrate on which the bipolar transistor is formed when an overvoltage (charging from outside due to static electricity or the like) is applied to the CMOS inner circuit.

In order to reduce the aforementioned phenomena of electric current concentration and electric field concentration on the surface of the semiconductor substrate, the inventor of the present invention has used a vertical bipolar transistor formed in a depth direction of the semiconductor substrate. By discharging an overvoltage applied to the CMOS inner circuit into a depth direction of the semiconductor substrate, the electrical current concentration and electric field concentration on the surface of the semiconductor substrate are avoided.

Each of the references cited in the Official Action teach a lateral bipolar transistor that discharge electric current along the surface of the semiconductor. None of these references teach or suggest a vertical bipolar transistor discharging an accumulated electric charge in a direction from a surface of the semiconductor substrate to a depth of the semiconductor substrate.

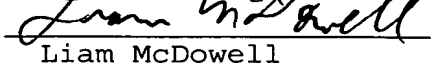
Accordingly, it is believed that the new claims avoid the rejections under §102 and §103 and are allowable over the art of record.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

Attached hereto is a marked-up version showing the changes made to the abstract and specification. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

YOUNG & THOMPSON

By 

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"VERSION WITH MARKINGS TO SHOW CHANGES MADE"

ABSTRACT OF THE DISCLOSURE

The Abstract of the Disclosure has been amended as follows:

To [make] reduce electric current concentration and electric field concentration [hardly take place] in junction parts even in the case of [performing] miniaturization, and to achieve triggering at low voltage[. An] , an ESD protection apparatus is installed between an input terminal [6] of a semiconductor integrated circuit chip and a CMOS transistor [100 and]. The ESD protection apparatus includes a trigger element [310 comprising] having diodes [311, 312] which are broken down by overvoltage applied to the input terminal [6] and an ESD protection element [210] including [longitudinal] vertical bipolar transistors [211, 212] for discharging the accumulated electric charge of the input terminal [6] by being electrically [communicated] discharged owing to the breakdown of the diodes [311, 312].

IN THE SPECIFICATION:

Page 1, the paragraph, beginning on line 12, has been amended as follows:

--A conventional ESD protection apparatus in the CMOS

process generally protects a semiconductor integrated circuit using a MOSFET transverse parasitic bipolar transistor by releasing the electric current in the transverse direction (lateral direction) in a silicon substrate. On the other hand, the ESD protection apparatus has been required to be further miniaturized since the number of pins to be mounted on one chip has been increased sharply following the recent acute requirement of development of semiconductor integrated circuits made finer.

Page 2, the paragraph, beginning on line 16, has been amended as follows:

--The ESD protection apparatus of the present invention is to be installed between a pad of a semiconductor integrated circuit chip and an inner circuit of the semiconductor integrated circuit chip. The ESD protection apparatus is provided with a trigger element comprising a diode to be broken down by overvoltage applied to the pad and an ESD protection element comprising a longitudinal bipolar transistor also known in the art as a vertical bipolar transistor for discharging the accumulated electric charge of the pad by being electrically [communicated] discharged attributed to the breakdown of the diode [(claim 1)].--

Page 3, the paragraph, beginning on line 9, bridging pages 3 and 4, has been amended as follows:

--A first practical example of an ESD protection apparatus of the present invention is as follows [(claim 3)]. The pad is an input terminal or an output terminal. The trigger element comprises a first and a second diodes and a first and a second resistors. The ESD protection element comprises NPN type first and second longitudinal bipolar transistors. Regarding the first diode, the cathode is connected with the pad and the anode is connected with the base of the first longitudinal bipolar transistor. Regarding the second diode, the cathode is connected with an electric power source terminal and the anode is connected with the base of the second longitudinal bipolar transistor. The first resistor is connected between the anode of the first diode and the ground terminal. The second resistor is connected between the anode of the second diode and the pad. Regarding the first longitudinal bipolar transistor, the collector is connected with the pad and the emitter is connected with the ground terminal. Regarding the second longitudinal bipolar transistor, the collector is connected with the electric power source terminal and the emitter is connected with the pad. Incidentally, at least either of a first diode, a first resistor and a first longitudinal bipolar transistor or a second diode, a second resistor and a second longitudinal bipolar transistor may be provided [(the same

is applied also for other claims)].--

Page 4, the paragraph, beginning on line 4, has been amended as follows:

--A second practical example of an ESD protection apparatus of the present invention is as follows [(claim 5)]. The pad is an electric power source terminal. The longitudinal bipolar transistor is NPN type. Regarding the diode, the cathode is connected with the pad and the anode is connected with the base of the longitudinal bipolar transistor. A resistor is connected between the anode of the diode and a ground terminal. Regarding the longitudinal bipolar transistor, the collector is connected with the pad and the emitter is connected with the ground terminal.--;

the paragraph, beginning on line 13, has been amended as follows:

--An ESD protection apparatus of the present invention may has the following constitution [(claim 11)]. The trigger element comprises, as a diode to be broken down by overvoltage applied to the pad, a first longitudinal bipolar transistor whose collector and base work and which discharges the accumulated electric charge of the pad by being electrically [communicated] <u>discharged</u> attributed to the breakdown of the diode. The ESD

protection element comprises a second longitudinal bipolar transistor for discharging the accumulated electric charge of the pad by being electrically [communicated] discharged attributed to the breakdown of the diode.--;

the paragraph, beginning on line 23, bridging pages 4 and 5, has been amended as follows:

--Practical examples of this case are as follows [(claims 12, 13)]. The pad is an input terminal or an output terminal. The trigger element comprises an NPN type longitudinal bipolar transistor A and an NPN longitudinal bipolar transistor B working as the first longitudinal bipolar transistor and a first and a second resistors. The ESD protection element comprises an NPN type longitudinal bipolar transistor C and an NPN type longitudinal bipolar transistor D working as the second longitudinal bipolar transistor. Regarding the longitudinal bipolar transistors A, C, the collectors are connected with the pad and the bases are connected with each other and the emitters are connected with a ground terminal. The first resistor is connected between the bases of the longitudinal bipolar transistors A, C and the ground terminal. Regarding the longitudinal bipolar transistors B, D, the collectors are connected with an electric power source terminal and the bases are

connected with each other and the emitters are connected with the pad. The second resistor is connected between the bases of the longitudinal bipolar transistors B, D and the pad [(claim 12)].--.

Page 5, the paragraph, beginning on line 13, has been amended as follows:

--The pad is an electric power source terminal. The first and second longitudinal bipolar transistors are NPN type and their collectors are connected with the pad and their bases are connected with each other and their emitters are connected with a ground terminal. A resistor is connected between the bases of the first and second longitudinal bipolar transistors and the ground terminal [(claim 13)].--;

the paragraph, beginning on line 20, has been amended as follows:

--The conductive types P and N may be taken as reverse conductive types N and P, respectively [(Claims 4, 6, 14 and 15)]. Even if the P and the N are reversed, the kind of a carrier alone is changed and naturally the same function can be realized. Incidentally, when the longitudinal bipolar transistor is taken as PNP type, the positions of the diode and the resistor are replaced with each other.--;

the paragraph, beginning on line 27, bridging

pages 5 and 6, has been amended as follows:

--The diode may comprise a single diode or plural diodes connected in series, the overvoltage may be an forward voltage for the diode and the breakdown may be a substantial breakdown by being electrically [communicated (Claims 2 and 7 to 10)] discharged. The diode forward descending voltage is, compared with the breakdown voltage, hard to depend on high impurity concentration and a low voltage. Consequently, by selecting the number of diodes to be connected in series, a desired substantial breakdown voltage can be accurately set.--.

Page 6, the paragraph, beginning on line 8, has been amended as follows:

--In the ESD protection apparatus according to [Claims 11,12,13 and 14 or 15)] the invention, the collector layers of the above described first longitudinal bipolar transistor and the above described second longitudinal bipolar transistor may be as simultaneously formed [(Claim 16)].--;

the paragraph, beginning on line 13, has been amended as follows:

--In the ESD protection apparatus according to [Claims 11,12,13 and 14 or 15] the invention, the above described first longitudinal bipolar transistor and the above described second

longitudinal bipolar transistor may have a common collector layer [(Claim 17)].--;

the paragraph, beginning on line 17, bridging pages 6 and 7, has been amended as follows:

--In the ESD protection apparatus according to [Claims 1, 2, 3, 5, 7, 9, 11 and 12 or 13] the invention, the longitudinal bipolar transistor or the diode comprises all or some of: a first N^-type well formed on the P type silicon substrate surface; a second N^-type well adjacent to this first N^-type well and formed on the P type silicon substrate surface; a second N^+layer formed on this second N^-type well surface; the P^-type well formed on the first N^-type well surface; the P^+layer and a first N^+layer formed on this P^-type well surface apart from each other; the insulation material installed between these P^+layer and the first N^+layer for preventing the electric connection with the P^+layer and the first N^+layer, wherein the second N^-type well and the P^-type well may be insulated by the insulation material for isolation and the P type silicon substrate and the P^-type well may be insulated by the insulation material for isolation [(Claim 18)]. In this case, the conductive type P and N may be taken as the reverse conductive N and P, respectively [(Claim 19)].--.

Page 7, the paragraph, beginning on line 6, has been

amended as follows:

--In the ESD protection apparatus according to [Claim 18] the invention, the P^+layer and the first and second N^+layers may be formed simultaneously with the P^+layer and the N^+layer of the CMOS transistor constituting the inner circuit [(Claim 20)]. [The same is also applied for the ESD protection apparatus according to Claim 19 (Claim 21).]--;

the paragraph, beginning on line 12, has been amended as follows:

--In the ESD protection device according to [Claim 18] the invention, a second N^-type well may be formed simultaneously with the N^-type well of the CMOS transistor constituting the inner circuit [(Claim 22)]. [The same is also applied for the ESD protection apparatus according to Claim 19 (Claim 23).]--;

the paragraph, beginning on line 17, has been amended as follows:

--In the ESD protection device according to [Claim 18 or Claim 19] the invention, the insulation material may be a dummy gate or a mere insulation material formed simultaneously formed with the gate electrode and the gate insulation film of the CMOS transistor constituting the inner circuit [(Claim 24)]. This dummy electrode or the insulation film may be formed in a ring shape on

the silicon substrate surface [(Claim 25)].--;

the paragraph, beginning on line 24, bridging pages 7 and 8, has been amended as follows:

--In the ESD protection apparatus according to [Claims 1, 2, 3, 5 and 7 or 9] the invention, the diode may [comprises] comprise: the N^-type well formed on the P type silicon substrate surface; the P^+layer and the N^+layer formed on the N^-type well surface apart from each other; and the insulation material formed in the inside from the above described P type silicon substrate surface between these P^+layer and N^+layer [(Claim 26)]. In this case, in the ESD protection apparatus according to [Claims 1, 2, 4, 6 and 8 or 10] the invention, the conductive type P and N may be the reverse conductive type N and P, respectively [(Claim 27)].--.

Page 8, the paragraph, beginning on line 5, has been amended as follows:

--In the ESD protection apparatus according to [Claims 1, 2, 3, 5 and 7 or 9] the invention, the diode comprises: the N^- type well formed on the P type silicon substrate surface; the P^- type well formed on this N^-type well surface; the P^+layer and the N^+layer formed on this P^-type well surface apart from each other; and the insulation material installed on the P type silicon

substrate surface between these P^+layer and N^+layer, wherein the P type silicon substrate and the P^-type well may be insulated by the insulation material for isolation [(Claim 28)]. In this case, in the ESD protection apparatus according to [Claims 1, 2, 4, 6 and 8 or 10] the invention, the conductive type P and N may be taken as the reverse conductive type N and P, respectively [(Claim 29)].--;

the paragraph, beginning on line 17, has been amended as follows:

--An ESD protection apparatus of the present invention may further have the following constitution [(claim 30)]. The diode comprises a P^- type well formed on the surface of a silicon substrate, an N^+ type layer and a P^+ type layer formed on the P^- type well surface at an interval from each other, and a dummy gate electrode formed on the P^- type well via an insulation film and between the N^+ type layer and the P^+ type layer and connected with a ground terminal. In this case, the electric field between the N^+ layer and the dummy gate electrode is intensified, the ESD trigger at a lower voltage. Incidentally, the conductive type P and N may be the reverse conductive type N and P, respectively [(Claim 31)].--.

Page 9, the paragraph, beginning on line 1, has been amended as follows:

--A method for fabricating an ESD protection apparatus relevant to the present invention is a method for fabricating an ESD protection apparatus according to [claim 1] the invention and comprises the following steps [(claim 32)]. (1) A first step of simultaneously forming an N^- type well of a CMOS transistor composing the inner circuit and an N^- type well for connector connection to be connected with the collector of the longitudinal bipolar transistor on a P type silicon substrate. (2) A second step of simultaneously forming a collector N^- type well to be a collector of the longitudinal bipolar transistor and an N^- type well of the diode on the P type silicon substrate. (3) A third step of simultaneously forming a P^- type layer to be a base in the collector N^- type well of the longitudinal bipolar transistor and a P^- type layer to be an anode in the N^- type well of the diode. (4) A fourth step of simultaneously forming an N^+ type layer in the P^- type well of the CMOS transistor, an N^+ type layer in the N^- type well for collector connection of the longitudinal bipolar transistor, an N^+ type layer to be an emitter in the P^- type layer of the longitudinal bipolar transistor, and an N^+ type layer to be a cathode in the P^- type layer of the diode. (5) A fifth step of simultaneously forming a P^+ type layer on the N^- type well of the CMOS transistor, a P^+ type layer on the P^- type layer of the

longitudinal bipolar transistor, and a P^+ type layer on the P^- type layer of the diode. In this case, the method for fabricating the ESD protection apparatus according to [Claim 2] the invention allows the anode and the cathode to be reversed [(Claim 33)].---.

Page 10, the paragraph, beginning on line 5, has been amended as follows:

--Further, the ESD protection apparatus fabrication method may further comprise a step of forming a dummy gate electrode simultaneously with a gate electrode of the CMOS transistor in the region where the collector N^- type well of the longitudinal bipolar transistor and N^- type well of the diode are formed in the second step (2). Incidentally, the dummy gate electrode is to prevent connection between the N^+ type layers of the longitudinal bipolar transistor and the diode formed in the step (4) and the P^+ type layers of the longitudinal bipolar transistor and the diode formed in the step (5) in the subsequent steps [(claim 34)]. Alternatively, the ESD protection apparatus fabrication method may further comprise a step of forming an insulation layer which prevents connection between the N^+ type layers of the longitudinal bipolar transistor and the diode formed in the step (4) and the P^+ type layers of the longitudinal bipolar transistor and the diode formed in the step (5) in the subsequent

steps [(claim 35)]. In the method for fabricating the ESD protection apparatus relevant to the present invention also, the conductive type P and N may be the reverse type N and P, respectively [(Claim 36)].--.

Page 12, the paragraph, beginning on line 21, has been amended as follows:

--FIG. 17 is a [plane] plan view of the ESD protection apparatus in Fig 16;--.

Page 14, the paragraph, beginning on line 18, bridging pages 14 and 15, has been amended as follows:

-- The ESD protection apparatus of this embodiment is installed between an input terminal (an input pad) 6 of a semiconductor integrated circuit chip and a CMOS transistor 100 and comprises a trigger element 310 comprising diodes 311, 312 which are broken down by overvoltage applied to the input terminal 6 and an ESD protection element 210 comprising longitudinal bipolar transistors 211, 212 for discharging the accumulated electric charge of the input terminal 6 by being electrically [communicated] discharged owing to the breakdown of the diodes 311, 312. Incidentally, FIG. 2 and FIG. 3 show only the longitudinal bipolar transistor 211 as some of ESD protection element 210 and only the diode 311 as some of the trigger element

310.--.

Page 15, the paragraph, beginning on line 3, has been amended as follows:

--The CMOS transistor 100 is a CMOS inverter comprising an NMOS transistor 101 and a PMOS transistor 102. Regarding the diode 311, the cathode is connected with the input terminal 6 and the anode is connected with the base of the longitudinal bipolar transistor 211. Regarding the diode 312, the cathode is connected with an electric power terminal 7 and the anode is connected with the base of the longitudinal bipolar transistor 212. A resistor 313 is connected with the anode of the diode 311 and a ground terminal 8. A resistor 314 is connected between the anode of the diode 312 and the input terminal 6. The longitudinal bipolar transistors 211, 212 are both NPN type. Regarding the longitudinal bipolar transistor 211, the collector is connected with the input terminal 6 and the emitter is connected with the ground terminal 8. Regarding the longitudinal bipolar transistor 212, the collector is connected with electric power terminal 7 and the emitter is connected with the input terminal 6. The resistors 313, 314 are made of a [singly] <u>single</u> crystal silicon, a polysilicon, a metal or the like formed in the same semiconductor integrated circuit chip.--;

the paragraph, beginning on line 21, bridging pages 15 and 16, has been amended as follows:

--Since today it has swiftly been [promote] promoted to make the gate insulation film of a CMOS transistor thinner, it is required for the ESD protection apparatus 210 [works] to work at a lower voltage [at] than that which the gate insulation film of the CMOS transistor 100 is broken. In this embodiment, the base potential of the longitudinal bipolar transistors 211, 212 is increased by voltage decreased at the time when the trigger current, which is the breakdown current of the diodes 311, 312, flows in the resistors 313, 314 to turn on longitudinal bipolar transistors 211, 212. Consequently, the large quantity of the electric charge attributed to the static electricity accumulated in the input terminal 6 is released in the longitudinal direction of the silicon substrate. As a result, electric current concentration can be prevented and a high ESD withstand level can be obtained.--.

Page 20, the paragraph, beginning on line 26, bridging pages 20 and 21, has been amended as follows:

--The ESD protection apparatus of this embodiment is installed between an electric power terminal (an electric power pad) 7 of a semiconductor integrated circuit chip and an inner

circuit 103 and comprises a trigger element 315 comprising a diode 316 to be broken down by overvoltage applied to the electric power terminal 7 and an ESD protection element 213 comprising a longitudinal bipolar transistor 214 for discharging the accumulated electric charge of the electric power terminal 7 by being electrically [communicated] discharged owing to the breakdown of the diode 316.--.

Page 23, the paragraph, beginning on line 13, has been amended as follows:

--The ESD protection apparatus of this embodiment is installed between an electric power terminal (an electric power pad) 7 of a semiconductor integrated circuit chip and an inner circuit 103 and comprises a trigger element 400 comprising a diode 402 to be broken down by overvoltage applied to the electric power terminal 7 and an ESD protection element 200 comprising a longitudinal bipolar transistor 201 for discharging the accumulated electric charge of the electric power terminal 7 by being electrically [communicated] discharged owing to the breakdown of the diode 402.--.

Page 27, the paragraph, beginning on line 27, bridging pages 27 and 28, has been amended as follows:

--The ESD protection apparatus of the present embodiment

is installed between an input terminal (an input pad) 6 of a semiconductor integrated circuit chip and a CMOS transistor 100 and comprises a trigger element 510 comprising diodes 511, 512 which are broken down by overvoltage applied to the input terminal 6 and an ESD protection element 210 comprising longitudinal bipolar transistors 211, 212 for discharging the accumulated electric charge of the input terminal 6 by being electrically [communicated] discharged owing to the breakdown of the diodes 511, 512. The diodes 511, 512 are a plurality of diodes connected in series, and the overvoltage is a forward voltage for the diodes 511, 512 and the breakdown is a substantial breakdown by being electrically [communicated] discharged. Incidentally, the diodes 511, 512 are illustrated in FIG. 26 as four diodes connected in series, but in FIG. 27 simplified and illustrated as two diodes connected in series for convenience's sake.--.

Page 30, the paragraph, beginning on line 9, has been amended as follows:

--If a trigger voltage of one stage portion of the diode is taken as Vf (about 0.6V), the trigger voltage Vf of the diodes of four stages connected in series is Vf x 4 = about 2.4V. When a surge of the ESD is applied to the pad and exceeds 2.4V, the forward series connection diodes are electrically [communicated]

discharged and inject the electric current into the base of the longitudinal bipolar transistor. By this trigger electric current, the longitudinal bipolar transistor which is a protection element of a high driving force starts operation, thereby discharging a charge of the ESD.--.

Page 31, the paragraph, beginning on line 6, has been amended as follows:

--The ESD protection apparatus of the present embodiment comprises a trigger element 515 comprising a diode 516 which is provided between the power source terminal 7 and the inner circuit 103 of the semiconductor integrated circuit and is broken down by overvoltage applied to an electric power source terminal 7, and an ESD protection element 213 comprising the longitudinal bipolar transistor 214 for discharging the accumulated electric charge of the electric power source terminal 7 by being electrically [communicated] discharged owing to the breakdown of the diode 516. The diode 516 is a plurality of diodes connected in series, and the overvoltage is a forward voltage for the diode 516 and the breakdown is a substantial breakdown by being electrically [communicated] discharged.--.

Page 32, the paragraph, beginning on line 27, bridging pages 32 and 33, has been amended as follows:

--In the diode comprising the P^+layers 2/the N well 5 as shown in FIG. 27, since a parasitic longitudinal bipolar transistor comprising the P^+ 2 layer/the N well 5/a P substrate 51 is formed, the electric current flowing into the P substrate 51 is generated. For this reason, the electric current to be supplied to the longitudinal bipolar transistor which is a protection element is reduced. However, in the present embodiment, since an N well 527 formed simultaneously with a collector layer 17 of an ESD protection element 210 exists, the diode comprising the N^+layer 521/the P^-layer 526 can prevent the electric current flowing in a longitudinal direction (depth direction of substrate), and therefore the electric current can be supplied to the base of the ESD protection element 210 with high efficiency (refer to FIG. 32). Consequently, according to the present embodiment, since a trigger electric current can be supplied to a base of the longitudinal bipolar transistor with high efficiency, the size of the trigger element can be reduced.--.